ABSTRACT OF THE DISCLOSURE

An equalizer consistent with certain embodiments has a differential analog tapped delay line made of a plurality of N series connected analog delay cells. Each cell has a pair of differential inputs and a pair of differential outputs. The delay line receives an input signal to be equalized. The differential input pair of the nth cell is connected to the differential output pair of the (n-1)th cell such that current is mirrored from the output pair to the input pair to form N-1 differential taps. Each one of N-1 differential input multiplying digital to analog converters (MDAC) is connected at its differential input at each differential tap, with each MDAC multiplying an analog signal at its input by a digital weighting factor to produce an output at a differential output. A differential slicer receives a sum of the differential outputs from each of the MDACs and produces an equalized output. This abstract is not to be considered limiting, since other embodiments may deviate from the features described in this abstract.